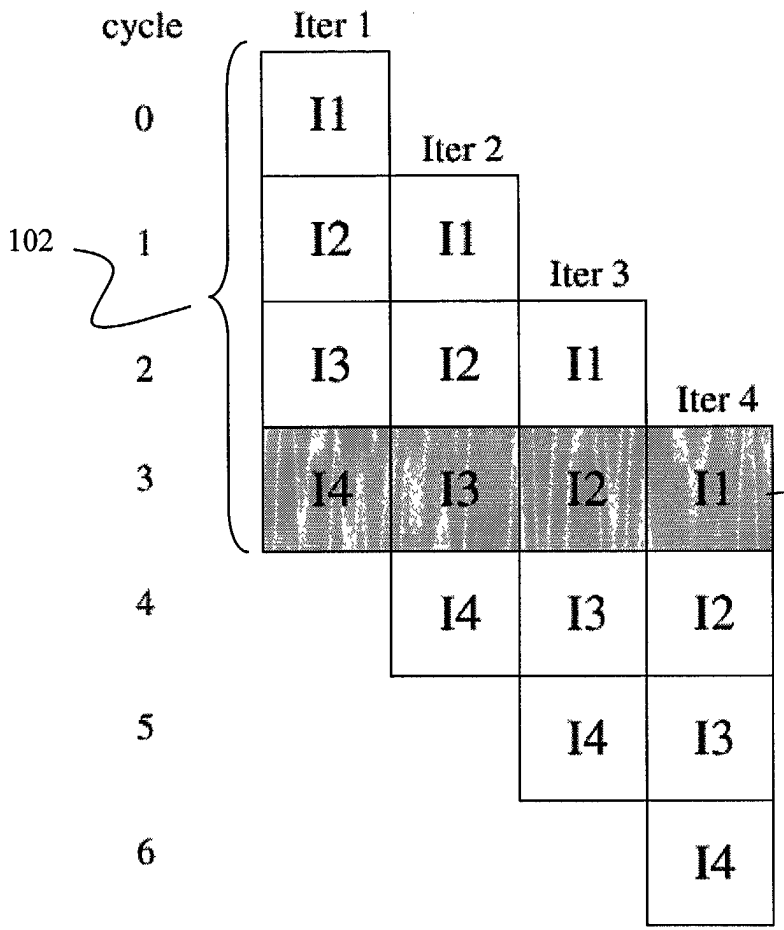

FIG. 1A

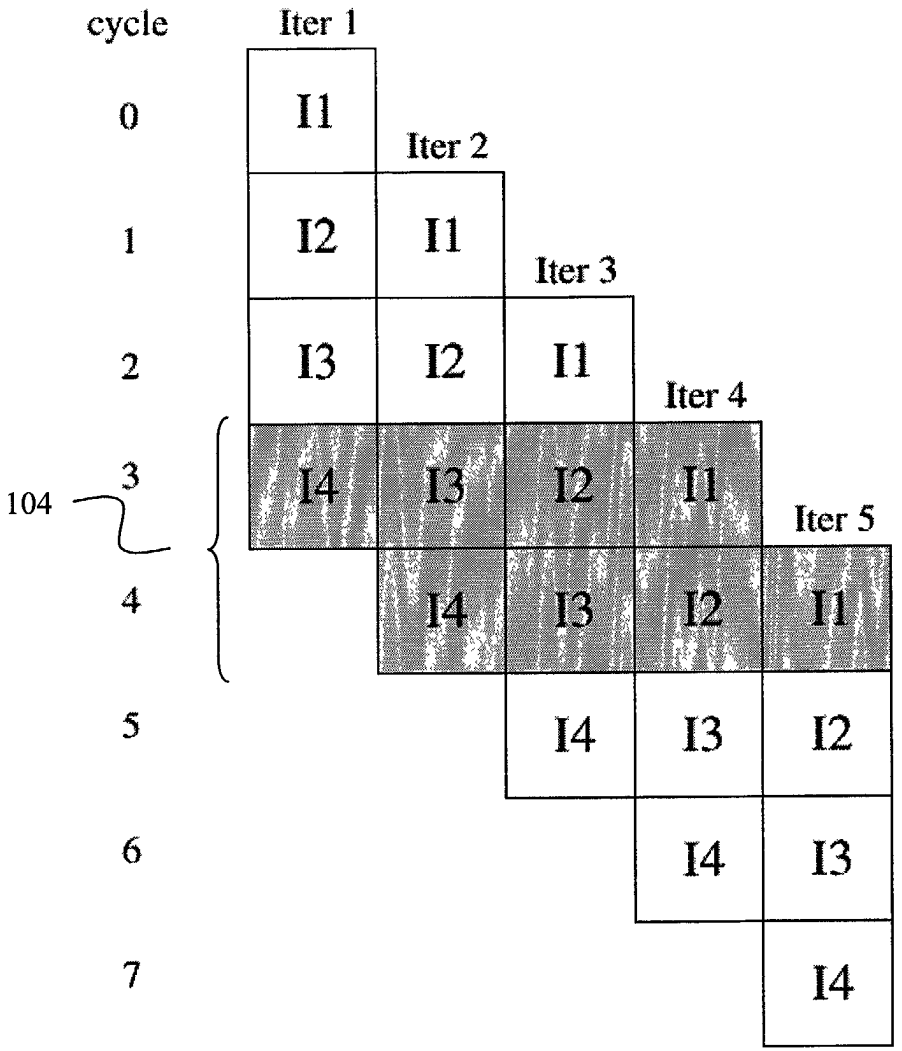

FIG. 1B

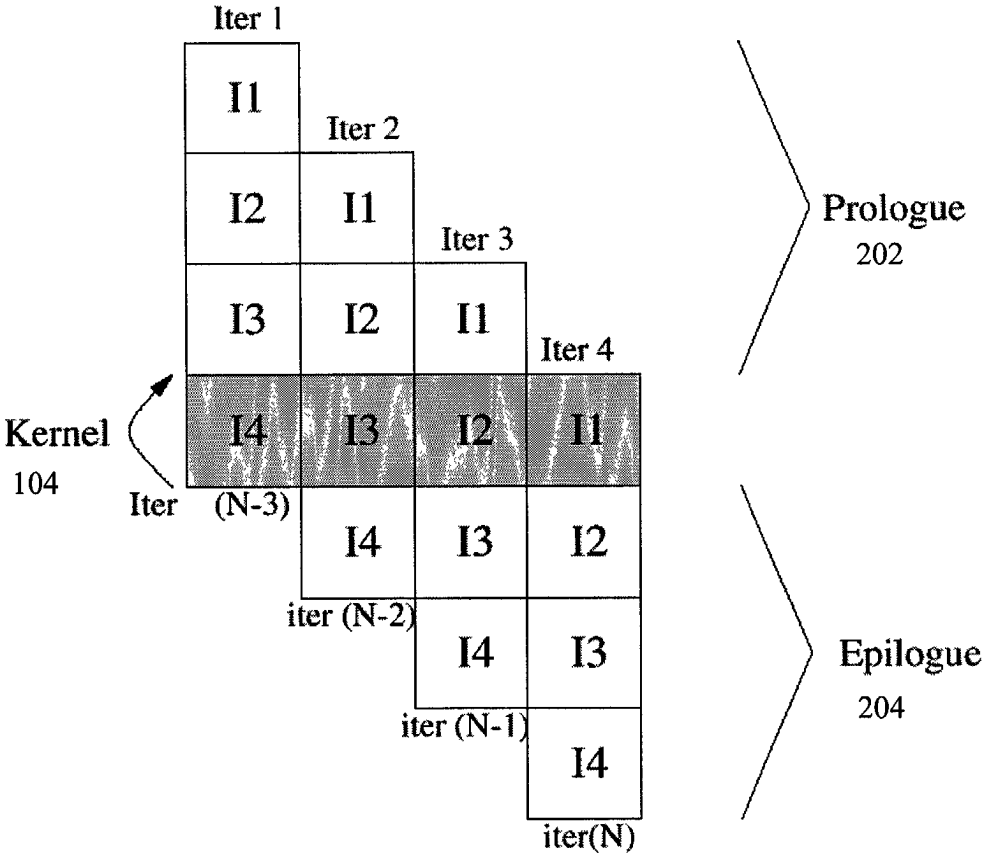

FIG. 2

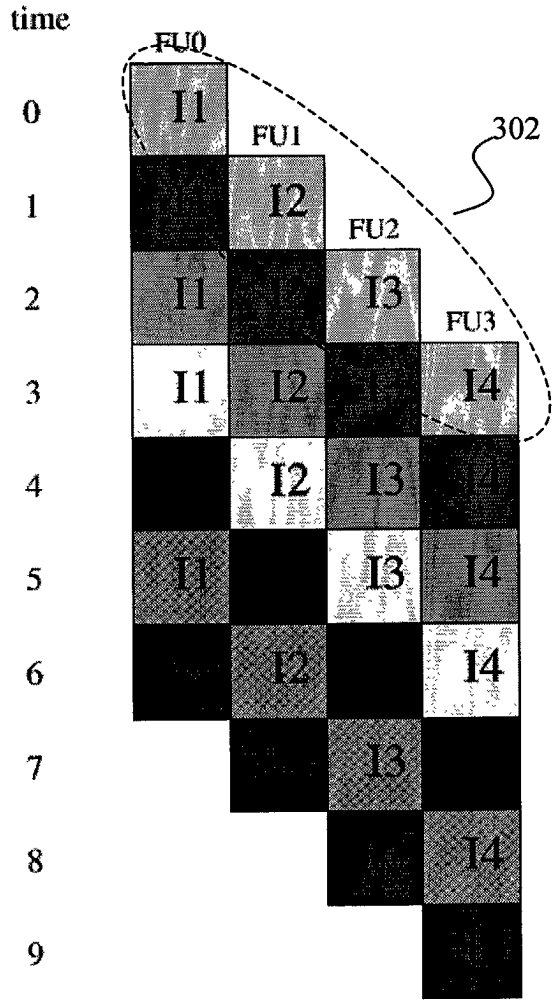

FIG. 3

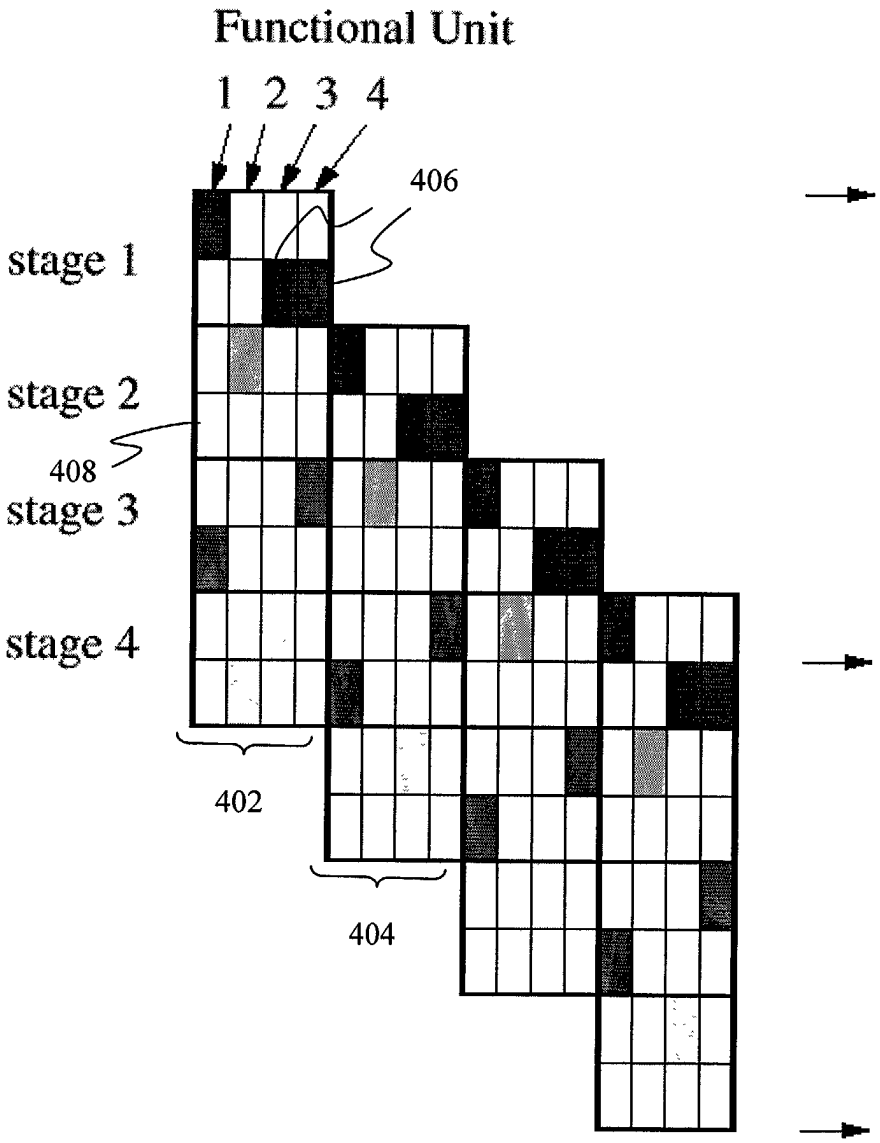

FIG. 4A

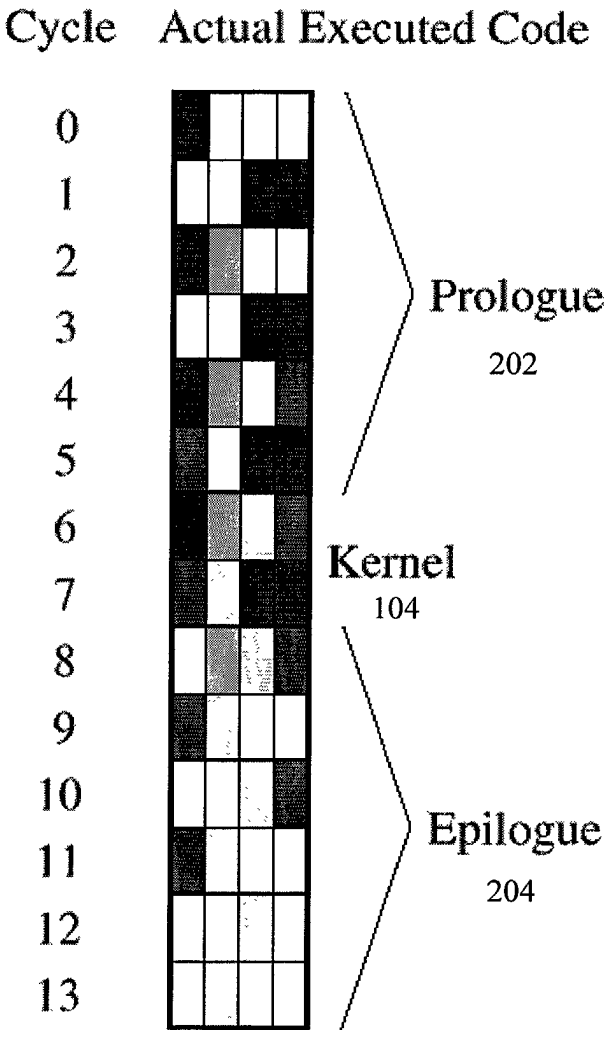

FIG. 4B

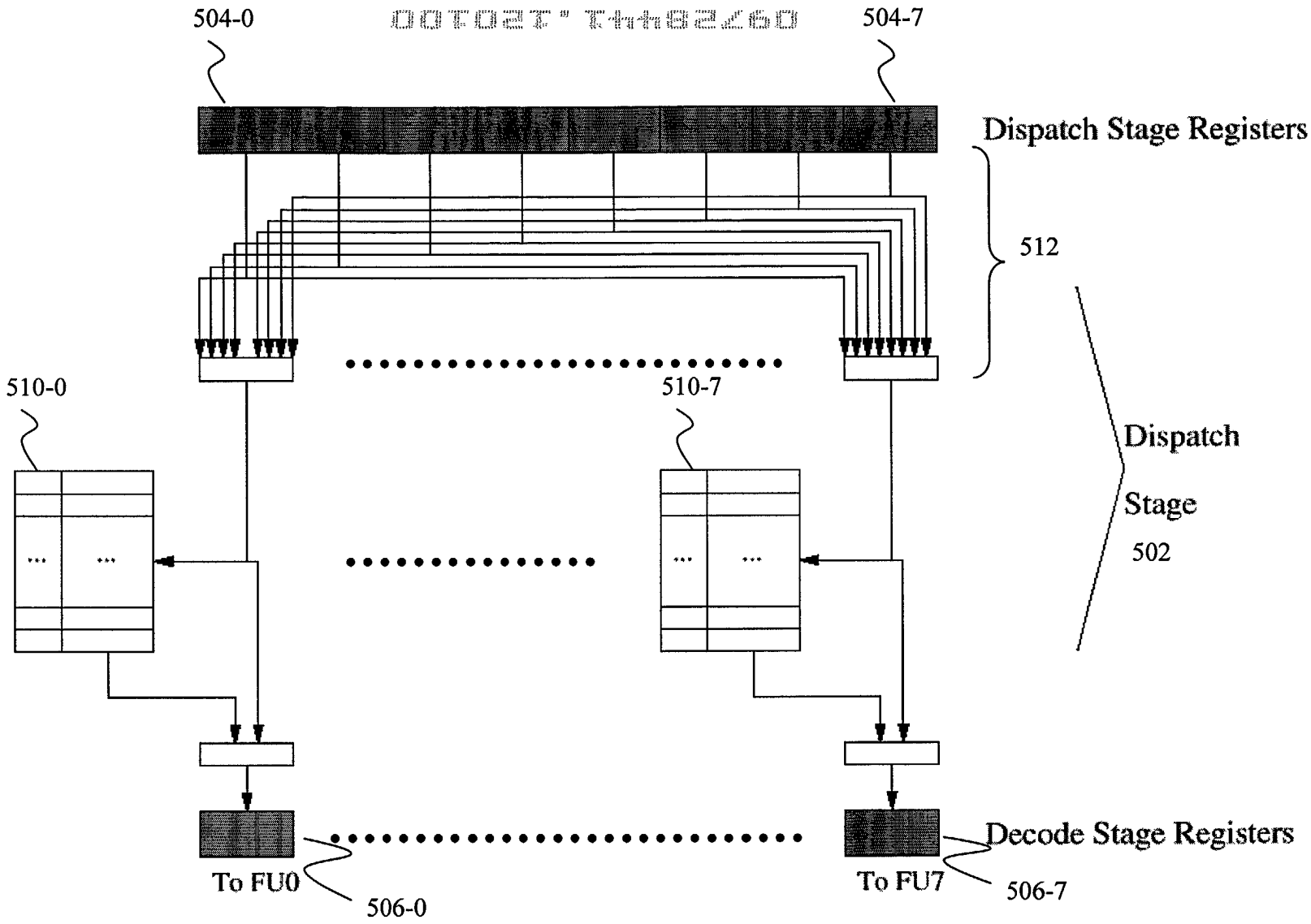
504-0
504-7
Dispatch Stage Registers
512
510-0
510-7
Dispatch
Stage
502
Decode Stage Registers
To FU0
506-0
To FU7
506-7

FIG. 5

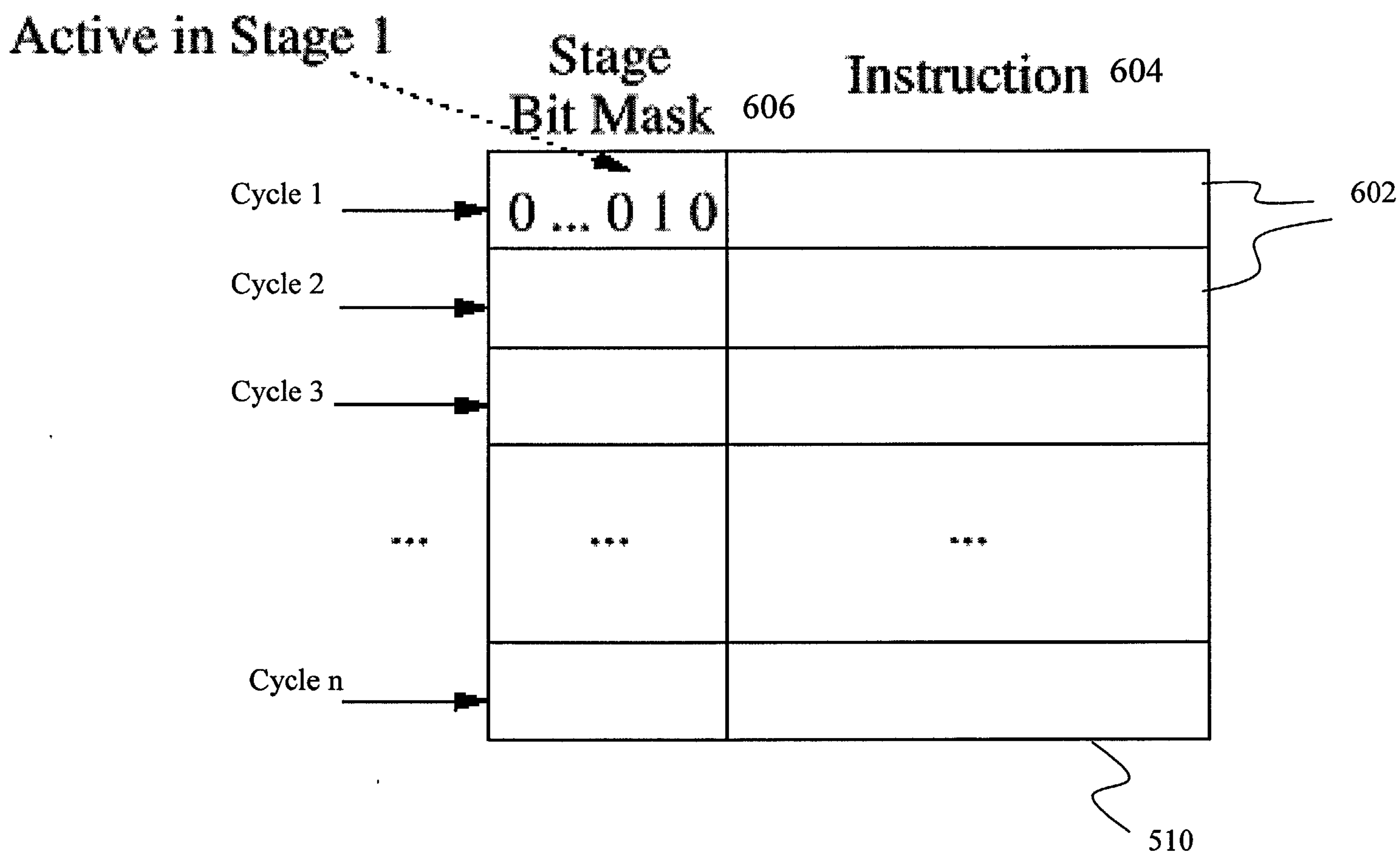

FIG. 6

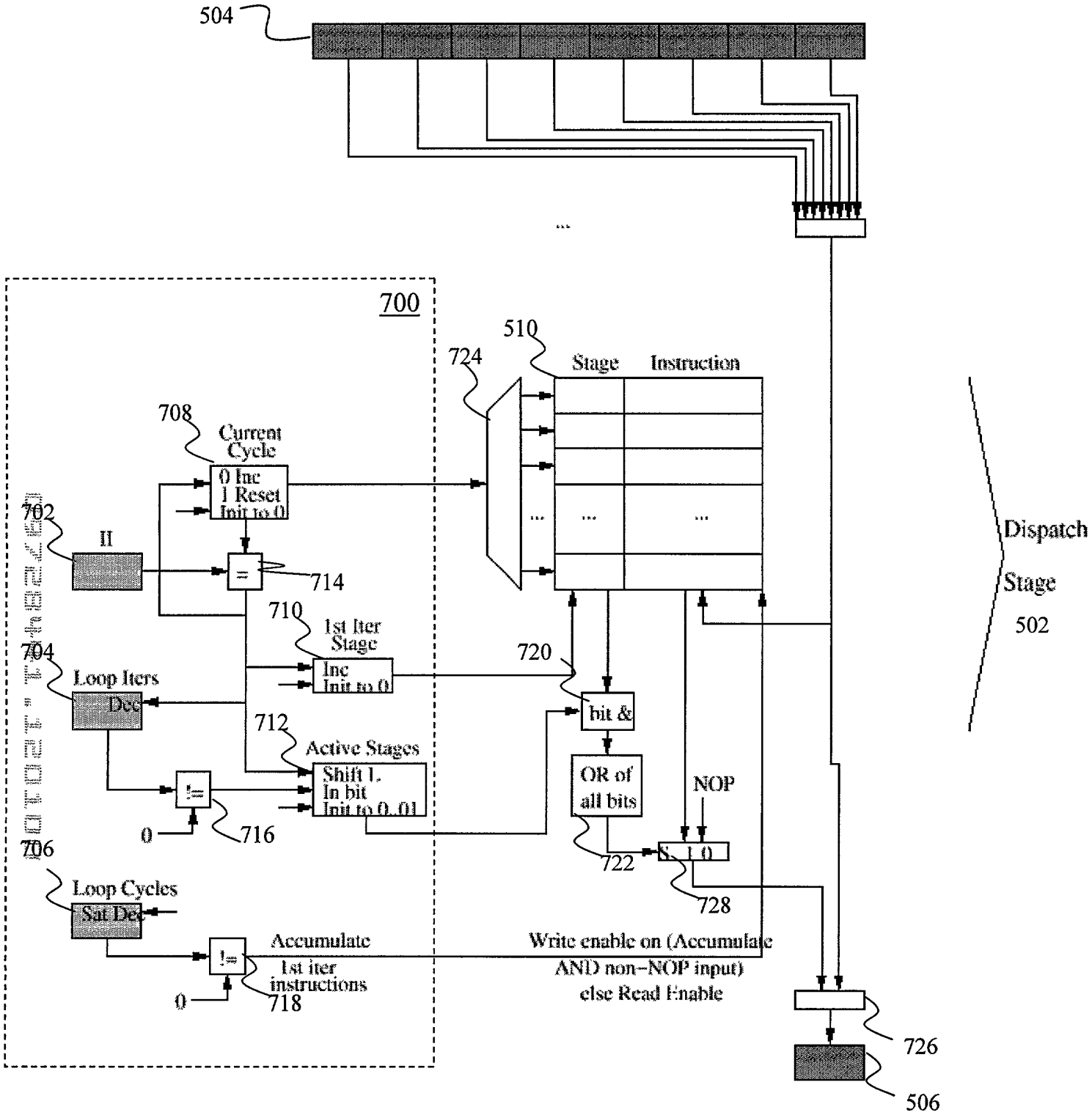
504
700
510
724
Stage
Instruction
708
Current Cycle
0 Inc
1 Reset
Init to 0
702
II
=
714
710
1st Iter Stage
Inc
Init to 0
704
Loop Iters
Dec
712
Active Stages
Shift L
In bit
Init to 0..01
!=
0
716
706
Loop Cycles
Sat Dec
!=
0
Accumulate
1st iter instructions
718
720
bit &
OR of all bits
NOP
722
728
Write enable on (Accumulate AND non-NOP input) else Read Enable
726
506
Dispatch Stage
502

FIG. 7

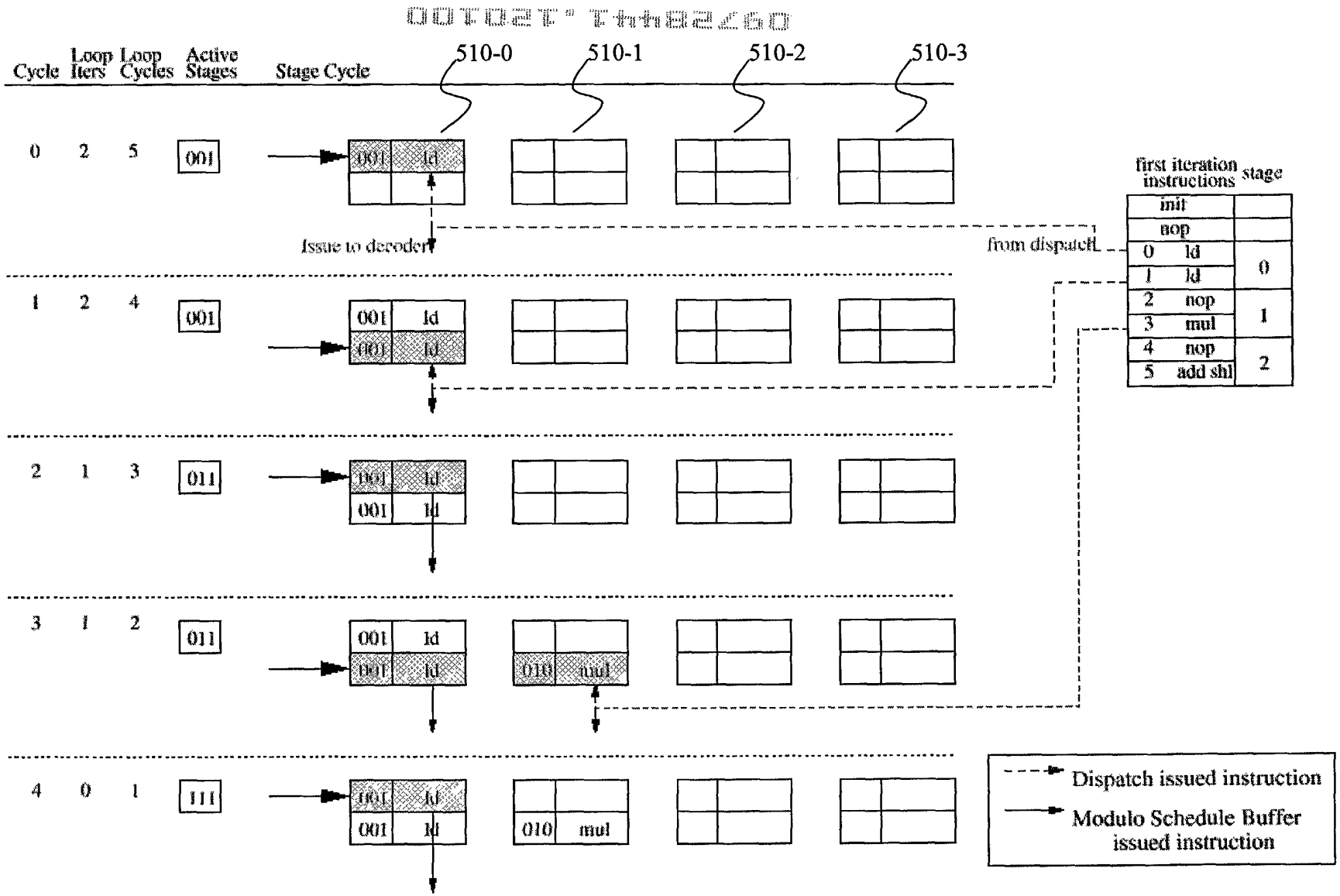
Cycle
Loop Iters
Loop Cycles
Active Stages
Stage Cycle
510-0
510-1
510-2
510-3
0 2 5 001
1 2 4 001
2 1 3 011
3 1 2 011
4 0 1 111
001 ld
010 mul
Issue to decoder
from dispatch
first iteration instructions
stage
init
nop
0 ld
1 ld
2 nop
3 mul
4 nop
5 add shl
0
1
2
Dispatch issued instruction
Modulo Schedule Buffer issued instruction

FIG. 8A

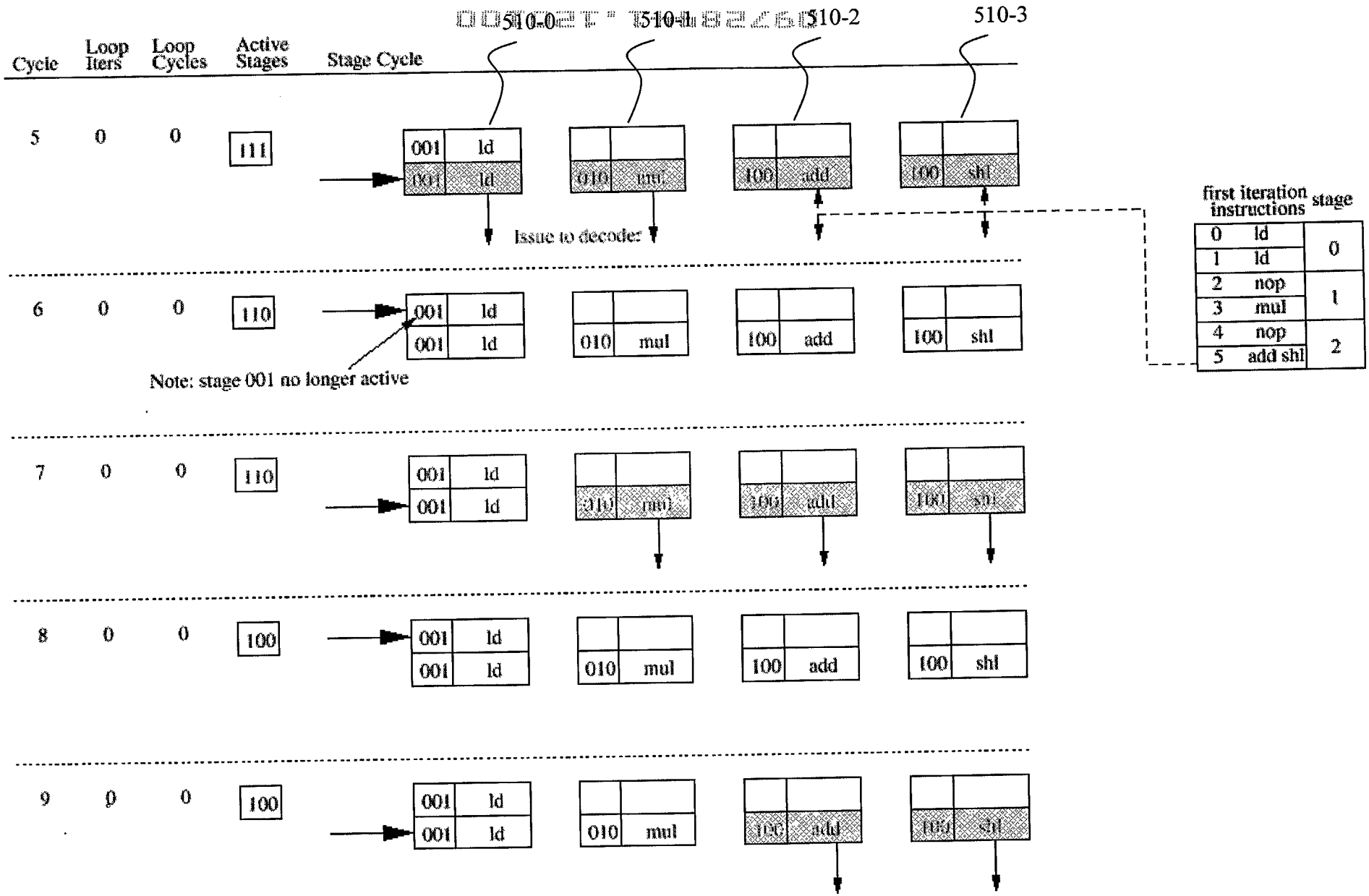
510-0
510-1
510-2
510-3
Cycle
Loop Iters
Loop Cycles
Active Stages
Stage Cycle
5 0 0 111
001 ld
001 ld
010 mul
100 add
100 shl
Issue to decoder
6 0 0 110
001 ld
001 ld
010 mul
100 add
100 shl
Note: stage 001 no longer active
7 0 0 110
001 ld
001 ld
010 mul
100 add
100 shl
8 0 0 100
001 ld
001 ld
010 mul
100 add
100 shl
9 0 0 100
001 ld
001 ld
010 mul
100 add
100 shl
first iteration instructions
stage
0 ld
1 ld
0
2 nop
3 mul
1
4 nop
5 add shl
2

FIG 8B

cycle	RTL
0	r1 <- 0
1	r1 <- r1 * 5
2	r1 <- r1 + 4
3	st [r2], r1
4	st [r3], r1

inst.	latency
mul	3
add	1

FIG. 9

EQ model or
LE model w/ actual
MUL latency of 3

cycle	RTL	
0	r1 <- 1	
1	r1 <- r1 * 5	
2	r1 <- r1 + 8	
3	st [r2], r1	; store 9 into [r2]
4	st [r3], r1	; store 5 into [r3]

FIG. 10A

EQ model w/ int. after cycle 2 or
LE model w/ actual
MUL latency of 2

cycle	RTL	
0	r1 <- 1	
1	r1 <- r1 * 5	
2	r1 <- r1 + 8	
3	st [r2], r1	; store 5 or 9 into [r2]
4	st [r3], r1	; store 5 or 9 into [r3]

FIG. 10B

EQ model w/ int. after cycle 1 or
LE model w/ actual
MUL latency of 1

cycle	RTL	
0	r1 <- 1	
1	r1 <- r1 * 5	
2	r1 <- r1 + 8	
3	st [r2], r1	; store 13 into [r2]
4	st [r3], r1	; store 13 into [r3]

FIG. 10C

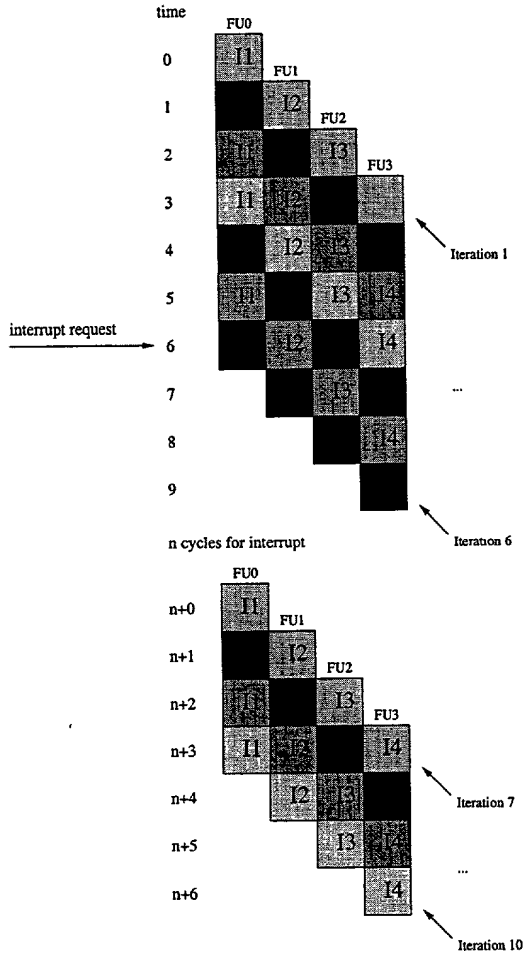

FIG. 11

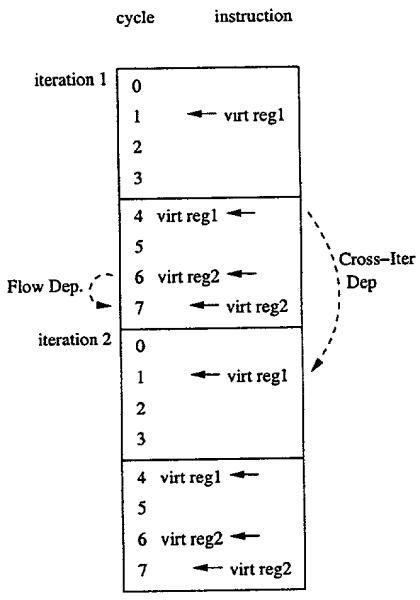

FIG. 12A

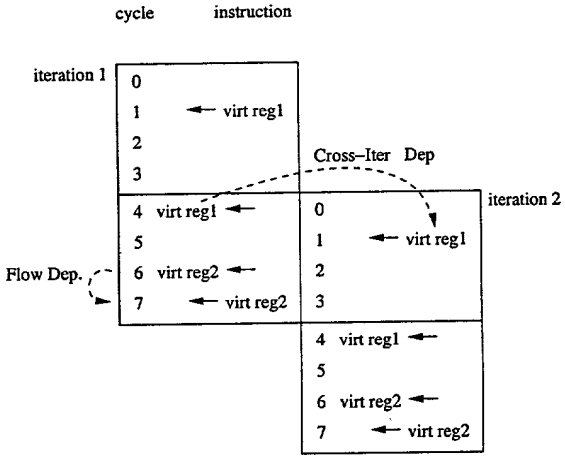

FIG. 12B

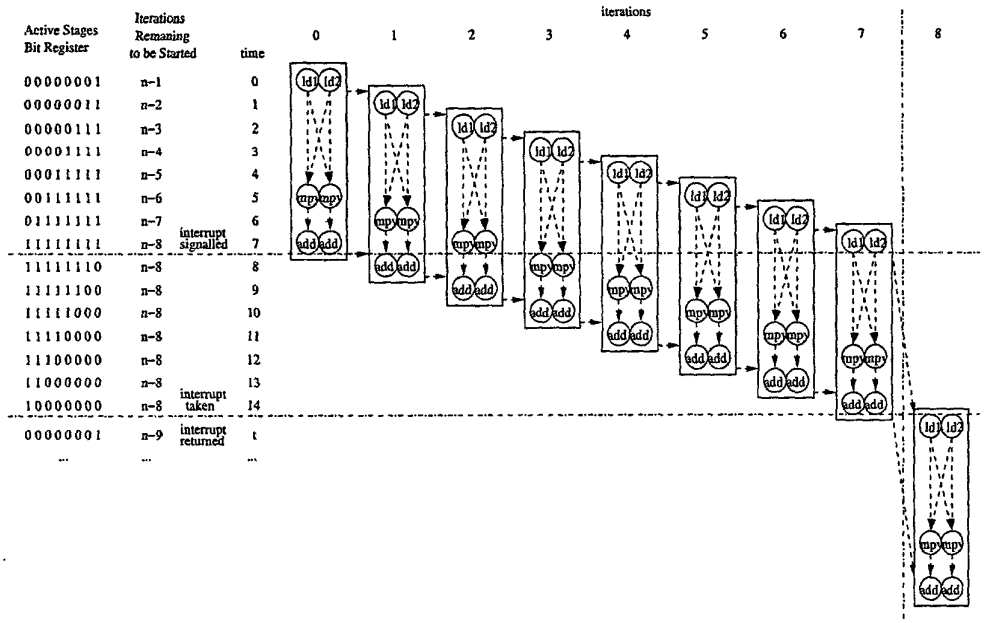

FIG. 13

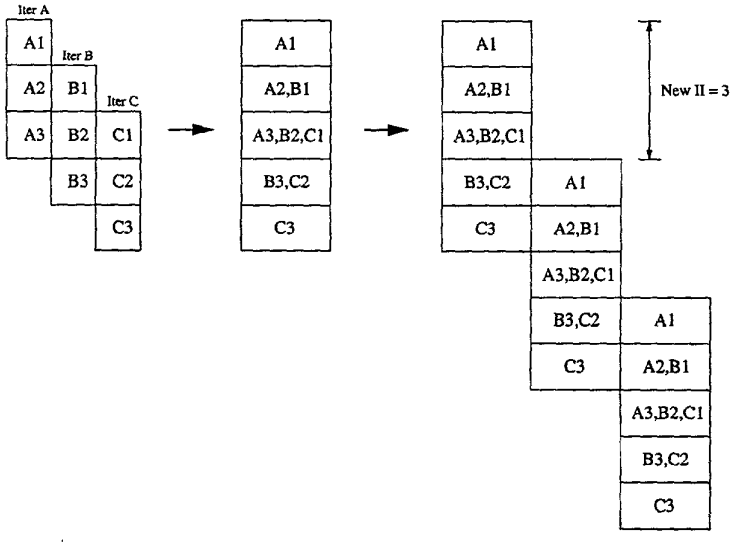

FIG. 14A FIG. 14B FIG. 14C